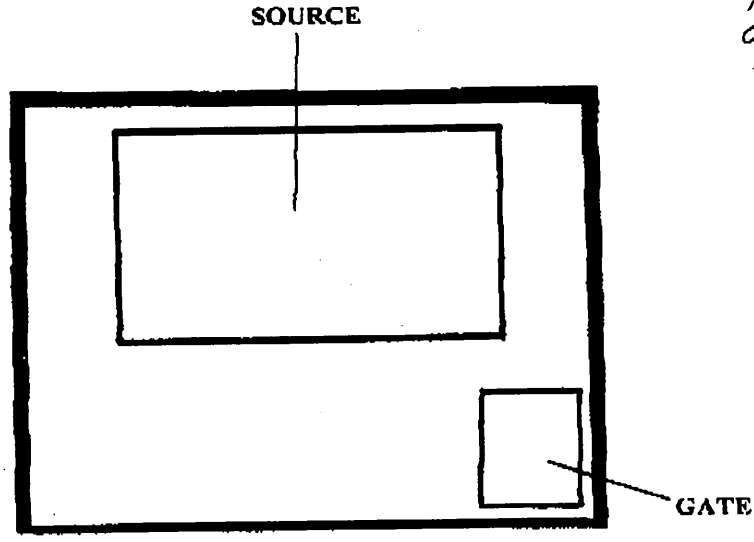
12/8/96

Dennis
layout of BUZ72A
as promised

Regards
Eric



CHIP BACK IS DRAIN

E & O E. Dice can be supplied to this layout only if it forms part of a specification or the chip identification, if below, is requested. Chip back potential is the level at which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated above. If no potential is given the chip back should be isolated. Nominal metallisation thicknesses are based on manufacturer's information. 1 mil. = 0.001 inch. Tolerance ±3 mils.

Approved	Metallisation Type	Metallisation Thickness (KÅ)	Chip Identification
	Top : Al		Line Source :
	Back : Ag		Mask Reference :
			Process :
	Back Potential : Drain		Version :
Date 12/08/96	Manufacturer's Part N° :		Geometry :

Chip Dimensions (mils.)	Bond Pads
100 x 95 x 9	S 67x 47 G 25x17

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